REMARKS

Claims 1-32 are pending in the present application. Claims 6, 7, 10, 17, 18, 21, 28, 29, and 32 were amended. Reconsideration of the claims is respectfully requested.

Amendments were made to the specification to correct errors in the abstract as requested by the examiner. No new matter has been added by any of the amendments to the specification.

Also, applicants have submitted formal drawings labeled Figures 1-5. These formal drawings address the 37 CFR 1.84 objection as noted by the examiner.

I. Objection to Claims 6-11, 17-22, and 28-32

The examiner has stated that claims 6-11, 17-22, and 28-32 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, the claims have been rewritten to overcome this objection.

II. 35 U.S.C. § 102, Anticipation, Claims 1-5, 12-16, and 23-27

The examiner has rejected claims 1-5, 12-16, and 23-27 under 35 U.S.C. § 102 as being anticipated by *Hass et al.*, (US Patent No. 6,330,977). This rejection is respectfully traversed.

With regard to claims 1, 12, and 23, the examiner states:

> Hass et al. disclose an electronic labeling systems and method and electronic card system and methods including the step of automatically detecting an insertion of an integrated circuit device into the receptacle device (see e.g. col. 10, lines 10-17) and in response to a detection of an insertion of the integrated circuit device into the receptacle device, automatically incrementing an insertion count (see e.g. col. 8, lines 46-56 and col. 62, lines 61-64)

Office Action, dated August 26, 2003, page 3.

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). The *Hass* reference cited by the examiner does not anticipate the present invention as recited in claim 1, because *Hass* fails to teach each and every element

of claim 1. Independent claim 1, which is representative of independent claims 12 and 23, reads as follows:

> 1. A method in a data processing system for automatically tracking insertions of integrated circuit devices into a receptacle device, said method comprising the steps of:
>
> automatically detecting, utilizing said data processing system, an insertion of an integrated circuit device into said receptacle device; and
>
> in response to a detection of an insertion of said integrated circuit device into said receptacle device, automatically incrementing an insertion count associated with said integrated circuit device, wherein said insertion count is used to track insertions of said integrated circuit device into said receptacle device.

Hass fails to teach the feature of automatically incrementing an insertion count associated with an integrated circuit device, wherein the insertion count is used to track insertions of the integrated circuit device into a receptacle device, as recited in claim 1 of the present invention. The examiner refers to the following sections of the *Hass* reference as evidence that *Hass* teaches this feature:

> A further point of the protocol is a way to reset the module. Suppose, for example, that a module is pulled out of the slot in the middle of a data transfer, so that the memory pointer inside the module shows that the next bit to be written is bit number 117. The next system into which this module is inserted must not assume that the module's starting address is necessarily zero.
>
> To make sure that the starting memory address of a newly inserted module is zero, as expected, the system sends a long string of write-zero commands, followed by a write-one command. The module contains simple sequential logic, which monitors the incoming bit stream for nonstop sequences of write-zero commands. If the module receives a nonstop sequence containing as many write-zero commands as the total length of the memory, the counter will freeze until the chip is reset. The chip will be reset if and only if an incoming "1" bit is seen while the counter is frozen.
>
> This provides a reset capability, whereby the system can ensure that the starting address of the module is accurately known. Thus, on every insertion of a new module, the system can send such a reset sequence to initialize the address pointer in the module. Note that this address-pointer-reset is only necessary once per insertion.

Hass, col. 8, lines 39-62.

> Another type of system uses modules 3100 similar to those of FIG. 29C, but with each module 3100 including a counter to keep track of the number of sensings., See FIG. 31A.

Hass, col. 10, lines 61-64.

The passages above teach a method for resetting a module, or integrated circuit, to ensure that, when the module is inserted into another system, the starting address of the module is accurate. These cited passages also teach that the module may include a counter to keep track of a number of sensings. However, there is no teaching in *Hass* of having an insertion count associated with the module and automatically incrementing the insertion count each time the module is inserted into a receptacle device. Instead, when transferring data between the system and the module, *Hass* teaches that there may be situations in which the inserted module may be pulled out of the slot, thus interrupting the data transfer. When the module is inserted into another system, the system may erroneously assume that the module's starting address is zero. Thus, Hass merely discloses that, in order to handle such a situation, upon every insertion of a new module, the system resets the memory pointer inside a module to indicate a memory address starting point of zero.

Furthermore, *Hass* uses a counter to "keep track of the number of sensings" (col. 62, line 63). Sensors are used in *Hass* for the sensing of external events, such as detecting the opening of a window or door, monitoring the temperature of the system, and tracking the movement of a mouse in a graphics display, as is described in the passages below:

> Preferred embodiment module **2900** includes features of modules **2400** and **2602** but also provides a third terminal for control or sensing of external events.

Hass, col. 61, lines 1-3.

> The distributed keypad of FIG. 29C can be used for various systems such as a burglar alarm: each sensor connects to a window or door, and when the window or door is opened, the adjacent module senses this and sets an internal flag which enables the presence detect when reset by the host.

Hass, col. 61, lines 30-35.

> A multitude of variously positioned and conditioned modules may be used to monitor the temperature of a complex system through a single wire.

Hass, col. 62, lines 3-5.

> Such a system could be used, for example, in a mouse for a graphic display system; the mouse rollers will drive two sensors, one for each planar direction, and two modules for each sensor (one for increasing and one for decreasing) will keep track of the distance moved by the mouse.

Hass, col. 62, line 65 to col. 63, line 3.

Thus, the counting mechanism in the module is used to monitor system events occurring outside of the module. There is no mention in *Hass* of using counters to count the number of times the module is inserted into the slot. Rather, *Hass* uses the counter in the module, when the module is already inserted into the system, to track system events external to the module.

In view of the above, *Hass* fails to teach each and every element of claim 1. Having a integrated circuit inserted into a receptacle and resetting the starting memory address, as well as using a counter in *Hass* to keep track of the number of sensings external to the integrated circuit does not teach the present invention's feature of automatically incrementing an insertion count associated with an integrated circuit device, wherein the insertion count is used to track insertions of the integrated circuit device into a receptacle device. As a result, the *Hass* reference fails to anticipate amended claims 1, 12, and 23 of the present invention.

Furthermore, *Hass* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Hass* actually teaches away from the presently claimed invention because it teaches keeping track of system events external to the integrated circuit while the IC is inserted into the system, as opposed to counting the number of times the integrated circuit is inserted into a receptacle as in the presently claimed invention. Absent the examiner pointing out some teaching or incentive to implement *Hass* and the feature of counting the number of times the integrated circuit is inserted into a receptacle, one of ordinary skill in the art would not be led to modify *Hass* to reach the present invention when the reference is examined as a

whole. Absent some teaching, suggestion, or incentive to modify *Hass* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the applicant's disclosure as a template to make the necessary changes to reach the claimed invention.

Applicants submit that independent claims 1, 12, and 23 are not taught by *Hass*. Claims 2-5, 13-16, and 24-27 are dependent claims depending on independent claims 1, 12, and 23, respectively. Applicants have already demonstrated claims 1, 12, and 23 to be in condition for allowance. Applicants respectfully submit that claims 2-5, 13-16, and 24-27 are also allowable, at least by virtue of their dependency on allowable claims.

Therefore, the rejection of claims 1-5, 12-16, and 23-27 under 35 U.S.C. § 102 has been overcome.

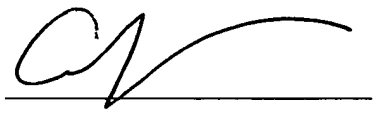
III. Conclusion

It is respectfully urged that the subject application is patentable over the cited reference and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 11/19/03

Respectfully submitted,



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